AMBA AXI/AHB/APB Bus and System Design and Verification

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Target audience and prerequisites
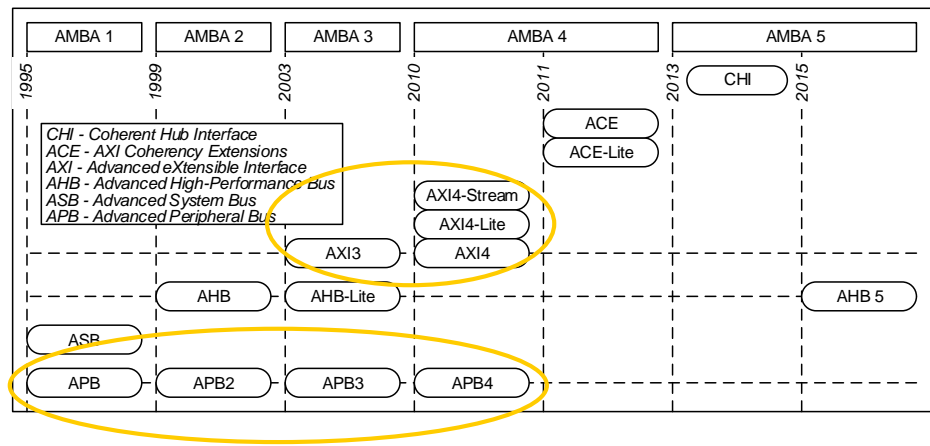
Target audience

- This lecture is prepared for engineers and students who are interested in developing IP based on AMBA AXI, AHB and APB.
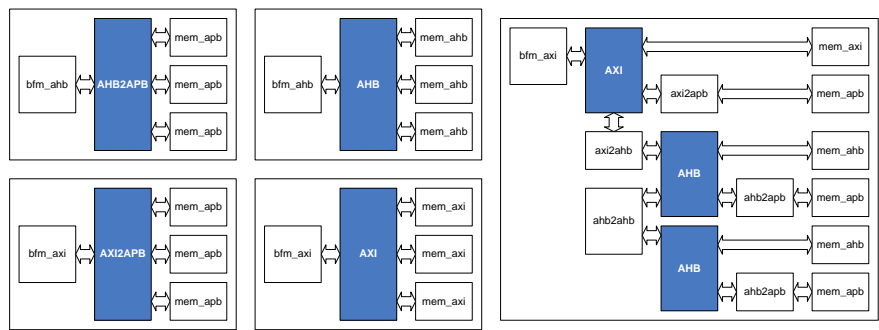
Prerequisites

- Basic knowledge of digital logic design
- Basic knowledge of the Verilog HDL language
- Basic knowledge of the C language
- Experience with industry standard HDL simulator such as ModelSim
- Experience with FPGA such as Xilinx and its development environment, i.e., ISE
- Experience with industry standard C compilation tool-chain such as Visual Studio and GNU GCC
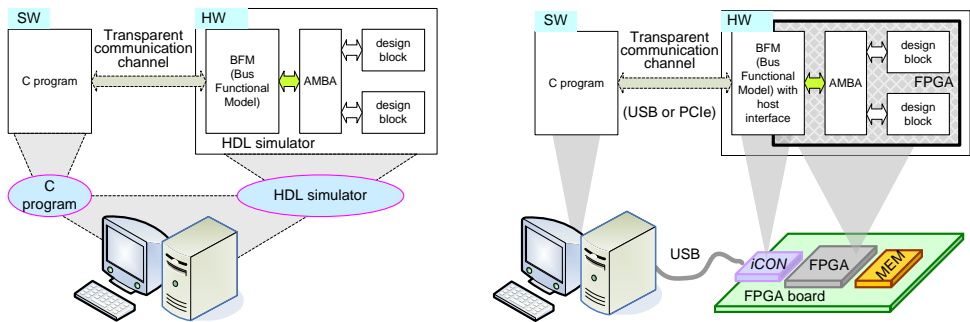- Experience with industry standard Operating Systems and text editor such as Windows/Linux and Vi/Vim.
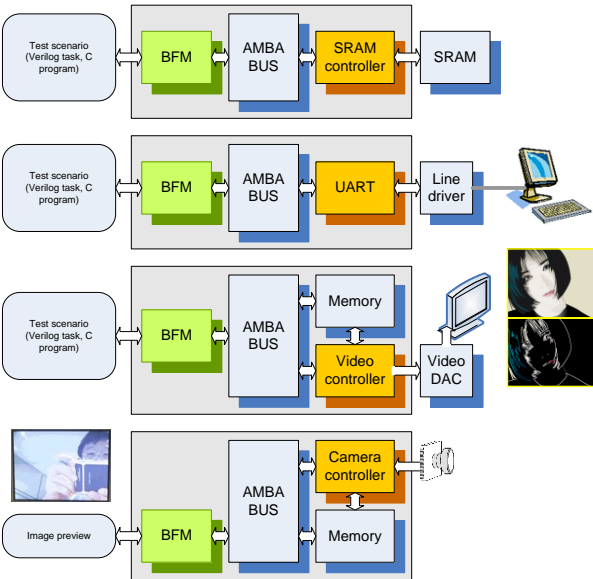
AMBA Bus

AMBA 1	AMBA 2	AMBA 3	AMBA 4	AMBA 5

1995 · 1999 · 2003 · 2010 · 2011 · 2013 · 2015

CHI

ACE
ACE-Lite

CHI - Coherent Hub Interface
ACE - AXI Coherency Extensions
AXI - Advanced eXtensible Interface
AHB - Advanced High-Performance Bus
ASB - Advanced System Bus
APB - Advanced Peripheral Bus

AXI4-Stream
AXI4-Lite
AXI3   AXI4

AHB   AHB-Lite   AHB 5

ASB

APB   APB2   APB3   APB4

AMBA

BFM with HW/SW Co-Simulation

Bus-based example designs

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