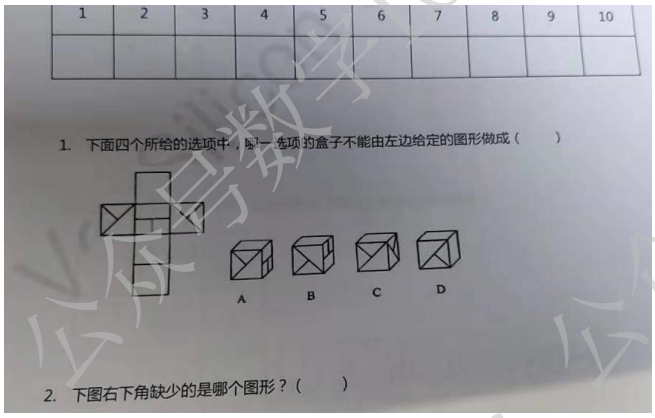
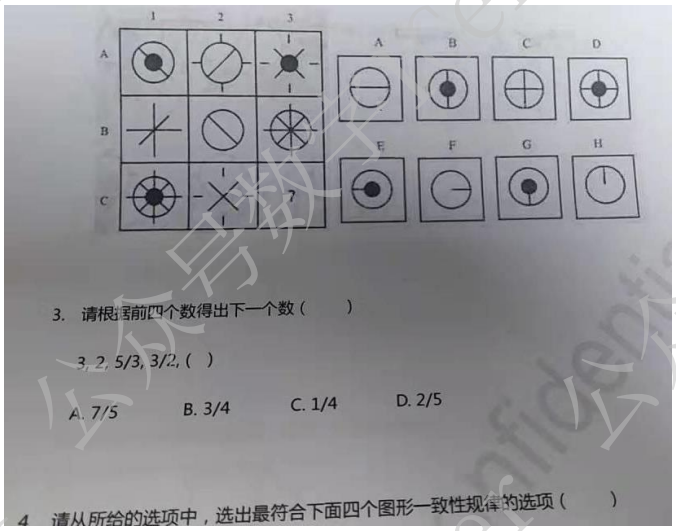
I. IQ test



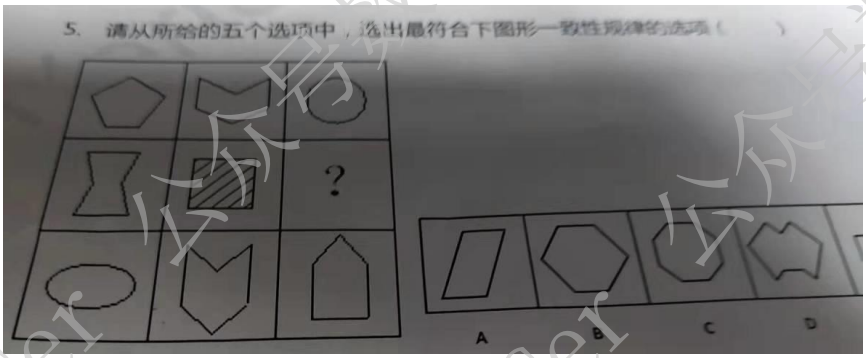
1.选 C



2.选 D，每行或每列相同的部分去掉，不同的部分保留

3.选 A

原数列 3, 2, 5/3, 3/2 可以变为 3/1, 4/2, 5/3, 6/4, 也就是分母 1、2、3、4，分子 3、4、5、6，所以下一个数 7/5。



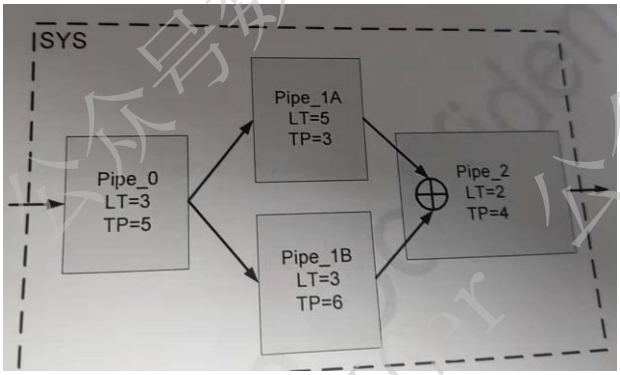
5.选 B，相对的位置稍做变换

II. **Basic Questions**

1. Choose at least 5 of below abbreviation to explain.
   CNN: 卷积神经网络 Convolutional Neural Networks
   ISP: 图像信号处理 Image Signal Processing
   FPGA:即现场可编程门阵列 Field Programmable Gate Array
   UVM: 通用验证方法学 Universal Verification Methodology
   ASIC: 专用集成电路 Application Specific Integrated Circuit
   DFT: 可测试性设计 Design for Testability
   STA: 静态时序分析 StaticTimingAnalysis

2. What is purpose of test coverage? What kinds of test coverage do you know? Please list the purpose and difference of each one.

3. Please describe the definition of throughput and latency. Please also calculate out the throughput and latency value of below pipeline system and show the detail step of calculation process.
   Assumption: Pipe_2 can only work when data from Pipe_1A and Pipe_1B both arrive.
   LT - stands for latency which is in unit of cycles.
   TP - stands for throughput which is in unit of bits/cycles.



4. Please write out the display content of below Verilog codes.

```
Integer A, B;
Initial begin
    A = 3; B = 4;
    #1;
    A <= 2; B <= A;
    $display ("CheckPoint1: A = %1d, B = %1d", A, B);
    #2;
    A<= B; B = A;
    $display ("CheckPoint2: A = %1d, B = %1d", A, B);
end
```

打印：3，4

打印：2，2

https://www.cnblogs.com/SYoong/p/5951670.html

答案： CheckPoint1: A = 3, B = 4 (这里要换行，display 换行)
CheckPoint2: A = 2, B = 2

注：根据时间点（#1 和#2）和优先级执行步骤，

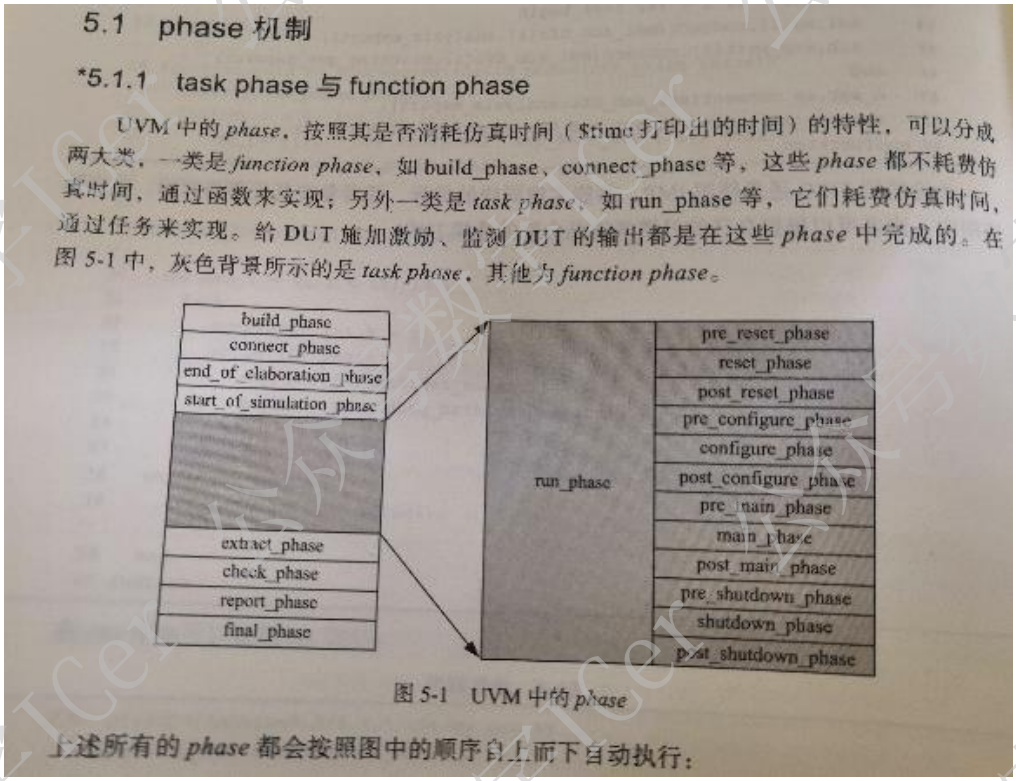
#0 时间点：A=3，B=4；

#1 时间点：由于 display 优先级比非阻塞赋值高，故先打印 A=3,B=4，再进行非阻塞赋值，A 为 2，B 为 3；

#2 时间点：阻塞赋值和 display 优先级相同，阻塞赋值语句在 display 之前，故先执行阻塞赋值 B 为 2，再执行 display，打印 A=2，B=2，最后进行非阻塞赋值 A 为 2；

5. UVM is an industry mainstream verification methodology for ASIC/SOC verification. Please list out all common phases of UVM.

UVM 实战 张强 p132

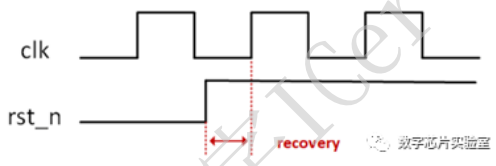


6. What are removal and recovery time constraints? Is asynchronous reset or synchronous reset beneficial to timing analysis?

对于一个异步复位寄存器来说，异步复位信号需要和时钟满足 recovery time 和 removal time 才能有效进行复位和复位释放操作，防止输出亚稳态。

Recovery time：恢复时间

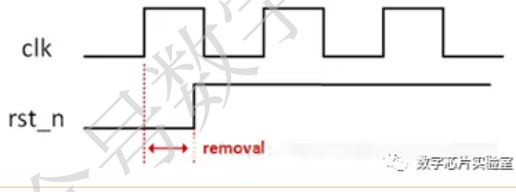
撤销复位时，恢复到非复位状态的电平必须在时钟有效沿来临之前的一段时间到来，才能保证有效地恢复到非复位状态，此段时间为 recovery time。类似于同步时钟的 setup time。



如图所示，rst_n 为 0 表示复位，clk 上升沿触发，rst_n 从 0 到 1 的上升沿与时钟上升沿之间地时间差必须不小于 recovery time 才能保证寄存器恢复到正常状态。

Removal time：撤销时间

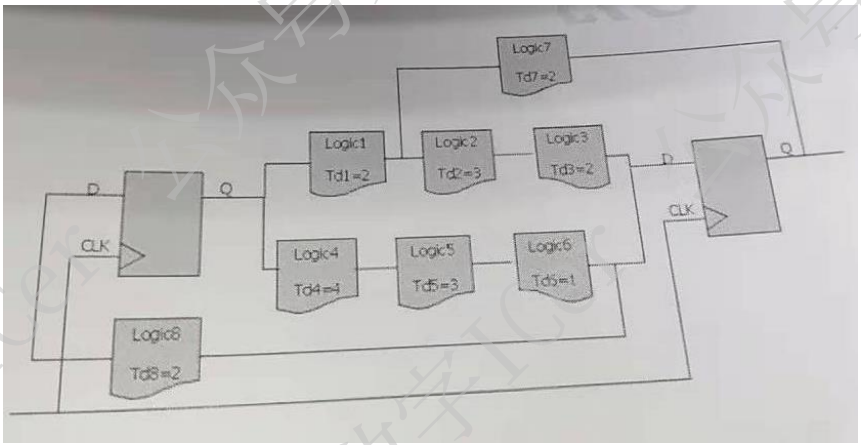
复位时，在时钟有效沿来临之后复位信号还需要保持的时间为去除时间 removal time。类似同步时钟 hold time。



如图所示，rst_n 为 0 表示复位有效，clk 为上升沿触发，rst_n 保持为 0 经过 clk 上升沿后仍需要保持一段时间，才能保证寄存器有效复位，防止亚稳态。

同步复位有利于时序分析（同步复位、异步复位优缺点，异步复位同步释放）

7. In below design, the delay assumption are as:
   (1) Clock period = 20 ns; (2) Clock uncertainty = 0.5ns; (3) Cell delay = 1.5ns;
   (4) FF setup = 1.1ns; (5) FF hold = 0.4ns;
   Please do:
   (a) Draw setup and hold critical path in picture.
   (b) Calculate setup slack T_{setup} and hold slack T_{hold}.



III. **Optional Technical Questions** (Plese only choose any **ONE QUESTION** to answer)

1. What is cache? What is the difference between write-back cache and write through cache? What is the advantage of write-back cache and write-through cache?

2. Why video/image encoders typically work on YUV color space not RGB color space? Could you list out the advantages of YUV color space?

3. If we want to design a SOC chip with below main components, please draw the SoC architecture diagram.
   AXI: ARM Cortex-A7, DMAC, Memory Controller
   AHB: SRAM, ROM, USB Controller

APB: UART, TIMER, WATCHDOG, I2C

群 PPT：SOC 框架

4. Please describe a typical interrupt handle flow, what does hardware do? What does software do? How to handle 2 or more interrupts nesting?

5. What is average filter, median filter, gaussian filter? For a 3*3 median filter, please draw the diagram and implement it in Verilog.

6. Please describe one FPGA project you have finished, including:
   (1) Why use FPGA for this project? What's the advantage of FPGA?
   (2) The detail FPGA part number and how many FPGA resources you have used.
   (3) Your FPGA design block diagram and relative peripherals.
   (4) The clock tree design in FPGA of your project.
   (5) If your design have one CPU, please describe the detail CPU bring up process, mempry map, interrupt and debug tools.
   (6) Any impressive issues you have faced and how to slove?

建议选择 1~2 个自己擅长的，面试可能会问